In the Specification:

Please replace paragraph **[0002]** with the following paragraph:

-- **[0002]** In a one-bit type EEPROM (electrically erasable programmable read only memory) cell, a device isolation layer 13 defining an active region and a device isolation region is formed in a substrate 11. A tunnel oxide 15 and a floating gate 17 are layered in the active region. In other words, the one-bit cell includes one floating gate per cell. The device isolation layer is formed through a LOCOS (local oxidation of silicon) or an STI (shallow trench isolation) process. --

Please replace paragraph **[0007]** with the following paragraph:

-- **[0007]** Referring to the example of Fig. 2a, a trench isolation layer 33 is formed in a silicon substrate 31. The trench isolation layer 33 defines an active region and a device isolation region in the substrate 31[[11]]. An oxide layer 35 (for the formation of a tunnel oxide) and a polysilicon layer 37 (for the formation of a floating gate) are then sequentially formed on the substrate 31 and the trench isolation layer 33. --